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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Kwan Ju KOH**, a citizen of the Republic of Korea, residing at Geumgangmaeul 407-101, Jung 4-dong, Wonmi-gu, Bucheon-si, Gyeonggi-do, Republic of Korea have invented new and useful **METHODS OF MANUFACTURING MOSFET DEVICES**, of which the following is a specification.

METHODS OF MANUFACTURING MOSFET DEVICES

TECHNICAL FIELD

[0001] The present disclosure relates to semiconductor devices and, more particularly, to methods of manufacturing metal oxide semiconductor field effect transistor (MOSFET) devices.

BACKGROUND

[0002] Generally, a gate of a MOSFET device is composed of a polysilicon material. Polysilicon is used because it satisfies a material feature required for a gate material, such as a high melting point, ease in forming a thin film and a line pattern, stability in an acidic environment, and a conformal surface thereof. Additionally, in an actual MOSFET device, the gate made of the polysilicon shows a low resistance because it contains a dopant such as, for example, phosphorous, arsenic, and/or boron.

[0003] However, as a level of integration of the MOSFET increases, there are limitations and drawbacks for implementing a resistance that is required between a narrow linewidth.

[0004] Using a conventional method for manufacturing a MOSFET device, it is difficult to form an ultra shallow junction that is required to a highly integrate MOSFET devices. Therefore, MOSFET fabrication requires a process technology to form an elevated source/drain region. Further, a control of a threshold voltage cannot be stabilized in the MOSFET device due to transformation of an implanted dopant array by an accompanying heat process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figs. 1A to 1H illustrate an example disclosed procedure for manufacturing MOSFET devices.

DETAILED DESCRIPTION

[0006] Referring to Fig. 1A, a shallow trench isolation (STI) 12 is selectively formed in an upper portion of a silicon substrate 10.

[0007] Referring to Fig. 1B, after a surface of an active area of the substrate 10 is oxidized to form an oxide layer 14, a dopant is lightly implanted to thereby form a lightly doped drain (LDD) around the active area of the substrate 10. Herein, a density of LDD can be varied.

[0008] Referring to Fig. 1C, a nitride layer 16 is deposited on an entire surface of a structure of Fig. 1B. Areas of the nitride layer 16 and the oxide layer 14 where a gate will be located are removed, and the substrate 10 corresponding to the area is also etched by a predetermined depth. Herein, the substrate 10 is etched by about 200 angstroms to 1000 angstroms in depth so that a hole for the gate is formed.

[0009] Referring to Fig. 1D, the exposed portion of the substrate 10 in the hole for the gate is oxidized at about 600 to 800 °C to form an oxide layer 18 having a thickness of about 100 angstroms. Ions are then implanted through the oxide layer 18 into the substrate 10. The oxide layer 18 prevents the substrate 10 from being damaged during the ion implanting for control of a threshold voltage.

[0010] Referring to Fig. 1E, the oxide layer 18 is removed and a gate insulating layer 20 is deposited over all the surface of the structure. Then the hole of the structure is filled with a polysilicon 22.

[0011] Referring to Fig. 1F, a chemical mechanical polishing process is performed until the nitride layer 16 is exposed. In the result, a polysilicon gate 23 filling the hole for the gate is formed.

[0012] Referring to Fig. 1G, the nitride layer 16 is removed by a wet etch and then an oxide layer 24 is formed thereon. Thereafter, a nitride layer is deposited on the oxide layer 24 and then etched back to form a gate sidewall 26 around the polysilicon gate 23.

[0013] Referring Fig. 1H, ions are implanted to form a source 28 and a drain 30 at both sides of the polysilicon gate 23 and the oxide layer 24 exposed by the etch back is removed to complete a MOSFET device.

[0014] As described above, an ultra shallow junction may be forming by elevating a source/drain region. The disclosed process may be used to manufacture a non-volatile memory device that is appropriate to form a self-align flash memory.

[0015] As disclosed herein, one example method may include (a) selectively forming a shallow trench isolation in a substrate; (b) forming a first oxide layer on a surface of an active region of the substrate and implanting ions thereinto for forming a low doped drain in the active region; (c) forming a nitride layer; (d) removing a part of the nitride layer and the oxide layer where a gate will be located and etching the substrate corresponding to the part by a predetermined depth; (e) forming a second oxide layer over an exposed portion of the substrate; (f) implanting ions into the substrate; (g) removing the second oxide layer; (h) depositing a gate insulating layer

and a polysilicon; (i) polishing until the nitride layer is exposed; (j) removing the nitride layer, depositing an oxide layer conformally and depositing an nitride layer; (k) etching the nitride layer to form a gate sidewall of nitride; (l) implanting ions into the substrate to form a source and drain at both sides of the gate; and (m) removing an exposed oxide layer.

[0016] Although certain example methods have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.